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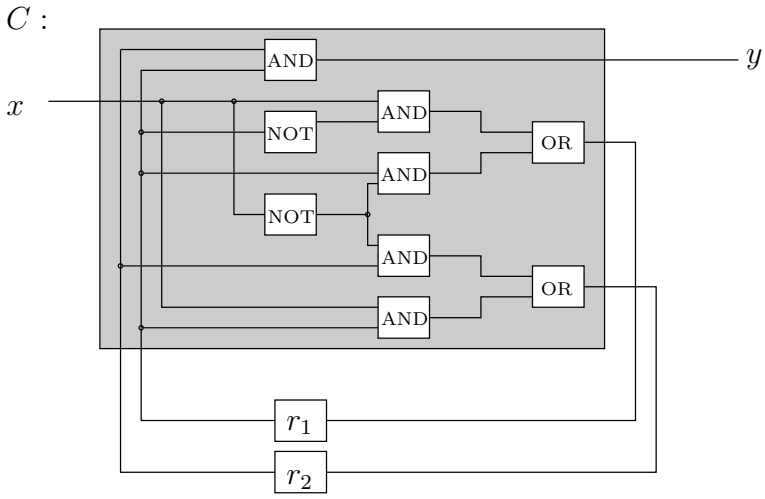
Introduction to Model Checking
Summer term 2007

– Series 1 –

Hand in on April 13 before the exercise class.

Exercise 1 (2 points)

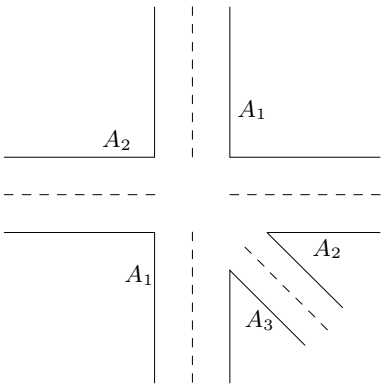
Consider the following sequential hardware circuit:

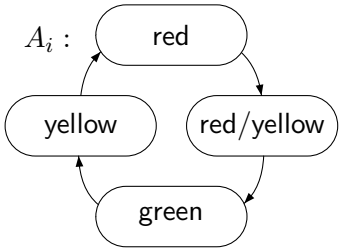


Give the transition system representation T of the circuit C.

Exercise 2 (1 + 1 + 2 points)

Consider the following street junction with the specification of a traffic light as outlined on the right.





a) Choose appropriate actions and label the transitions of the traffic light transition system accordingly.

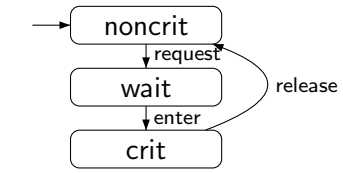
b) Give the transition system representation of a (reasonable) controller C that switches the green signal lamps in the following order: $A_1, A_2, A_3, A_1, A_2, A_3, \ldots$.
(*Hint: Choose an appropriate communication mechanism*)

c) Outline the transition system $A_1 \| A_2 \| A_3 \| C$.

Exercise 3 **(1 + 3 points)**

A concurrent system comprises $P_1, \ldots, P_n$ competing processes (without shared memory) that access common resources within their critical sections. We assume that the resources may only be accessed exclusively and that k equivalent instances are available.
Further, let $n, k \in \mathbb{N}$ with $2 \leq k \leq n$.
Process P_i can be described by a transition system $\mathcal{T}_i$ with three states and the actions $request, enter$ and $release$ as indicated on the right.

$\mathcal{T}_i$:



a) Develop a transition system representation of an arbiter that communicates with the processes using actions $request$ and $release$. The arbiter should assure that there are no more than k processes within their critical section at the same time.

b) Sketch the transition system of the parallel composition

$$(\mathcal{T}_1 ||| \mathcal{T}_2 ||| \mathcal{T}_3) \parallel_{Syn} Arbiter$$

with $Syn = \{request, release\}$ for $k = 2$. You need not consider the states $wait_i$.